REMARKS

In the Office Action, claims 16-33 are rejected under 35 U.S.C. § 102(b). Applicants respectfully submit that these rejections are improper at least for the reasons set forth below.

In the Office Action, claims 16-33 are rejected under 35 U.S.C. § 102. More specifically, claims 16-33 are rejected as being anticipated by U.S. Patent No. 6,600,160 ("*Kobayashi*"). The Patent Office alleges that *Kobayashi* discloses each feature of the claimed subject matter as defined in claims 16-33.

Of the pending claims at issue, claims 16, 22 and 28 are independent claims. Independent claim 16 recites a picture processing apparatus comprising a light receiving portion for generating an electric signal corresponding to an intensity of a received light; an amplifying portion for amplifying the electric signal generated by the light receiving portion; a plurality of storing portions, wherein each of the storing portions stores, as a current signal, the electric signal amplified by the amplifying portion; a load portion for converting the current signal stored by each of the storing portions into a voltage signal; a bias portion for supplying an offset current to an input of the load portion; a calculating portion for calculating an output signal of the load portion based on the voltage signal converted by the load portion; and an outputting portion for outputting a calculated result of the calculating portion. Claims 17-21 depend from claim 16 and thus, as a matter of law, incorporate each of the features of claim 16.

Independent claim 22 recites a plurality of pixels operable within a photographing device, the pixels arranged on a circuit in a matrix, for detecting a brightness of an object. Each of the pixels comprises a light receiving portion for generating an electric signal corresponding to an intensity of a received light; an amplifying portion for amplifying the electric signal generated by the light receiving portion; a plurality of storing portions, wherein each of the storing portions stores, as a current signal, the electric signal amplified by the amplifying portion; a load portion for converting the current signal stored by each of the storing portions into a voltage signal; a bias portion for supplying an offset current to an input of the load portion; a calculating portion for calculating an output signal of the load portion based on the voltage signal converted by the load portion; and an outputting portion for outputting a calculated result of the calculating portion. Claims 23-27 depend from claim 22 and thus, as a matter of law, incorporate each of the features of claim 22.

Independent claim 28 recites a photographing device for detecting a brightness of an object comprising a pixel area in which pixels are arranged in a matrix. Each pixel comprises a light receiving portion for generating an electric signal corresponding to an intensity of a received light and an amplifying portion for amplifying the electric signal generated by the light receiving portion; a second amplifying area in which second amplifying portions are arranged in each column of the matrix of the pixels in the pixel area, wherein each of the second amplifying portions amplifies a current signal based on current mirror amplification by a first mirror transistor and a second mirror transistor connected such that a gate electrode of the first mirror transistor faces a gate electrode of the second mirror transistor; a pixel-outside storing area in which a plurality of storing portions are arranged in a matrix corresponding to the arrangement of the pixels in the pixel area, wherein each of the storing portions stores, as a current signal, the electric signal that has been amplified; a load portion and calculating portion area in which a plurality of load portions and a plurality of calculating portions are arranged in each column of the matrix of the pixels of the pixel area, wherein each of the load portions converts the current signal of the corresponding storing portion into a voltage signal, and wherein each of the calculating portions performs a calculating process; and an outputting portion area in which a plurality of outputting portions are arranged in each column of the matrix of the pixels of the pixel area, wherein each of the outputting portions outputs a calculated result of the corresponding calculating portion. The pixel area, the second amplifying portion area, the pixel-outside storing area, the load portion and calculating portion area, and the outputting portion area are disposed on a circuit. Claims 29-33 depend from claim 28 and thus, as a matter of law, incorporate each of the features of claim 28.

In contrast to the claimed invention, Applicants believe that *Kobayashi* is deficient with respect to at least a number of features of the claimed invention. For example, Applicants believe that *Kobayashi* at least fails to describe a plurality of storing portions, wherein each of the storing portions stores, as a current signal, the electric signal amplified by the amplifying portion. Rather, *Kobayashi* discloses capacitors that accumulate signal charges sent directly from the photoelectric conversion element prior to being received by the amplifying MOS transistor. See, *Kobayashi*, column 2, lines 33-55 and Figs. 1 and 4. The photoelectric conversion element is connected directly to the gate of the MOS transistor. *Id.* In fact, if the

photoelectric conversion element has sufficient capacitance, the capacitor is not needed. See, *Kobayashi*, column 2, lines 48-51; column 5, lines 18-21. Thus, *Kobayashi* at least fails to describe a plurality of storing portions, wherein each of the storing portions stores, as a current signal, the electric signal amplified by the amplifying portion.

In addition, Applicants believe that *Kobayashi* at least fails to describe a load portion for converting the current signal stored by each of the storing portions into a voltage signal as required by the claimed invention. The Office Action alleges that the load portion for converting the current signal stored by each of the storing portions into a voltage signal is disclosed by the source follower circuit in *Kobayashi* at column 5, lines 34-38. The source follower circuit has a photoelectric conversion element, a source-follower input MOS and a vertical selection-switch MOS. See, *Kobayashi*, column 5, lines 18-30. The source follower circuit does not convert the current signal of the photoelectric conversion element into a voltage signal. Rather, when a signal voltage is generated at the gate of the source-follower input MOS corresponding to the electrical charges accumulated in the photoelectric conversion element, the source follower circuit reads the signal voltage with the current amplified. See, *Kobayashi* at column 5, lines 34-38. Thus, *Kobayashi* is deficient with respect to a load portion for converting the current signal stored by each of the storing portions into a voltage signal.

Further, *Kobayashi* is deficient with respect to a bias portion for supplying an offset current to an input of the load portion as required by the claimed invention. The Office Action alleges that the bias portion for supplying an offset current to an input of the load portion is disclosed in *Kobayashi* by the bias region where bias voltage (VDS) is equal to pinch-off voltage at column 12, lines 1-5. However, *Kobayashi* is only describing what the reset voltage V_{sig0} is expressed as when both the vertical selection switch 23 and the reset switch 24 operate in a pentode region (region in which the bias (VDS) between source and drain is equal to or lower than a pinch-off voltage). *Id.* Vertical selection switch 23 serves as a selection switch means for selecting each pixel, and reset switch 24 serves as a reset means for resetting the gate of an MOS transistor. See, *Kobayashi*, column 3, lines 35-45. Neither vertical selection switch 23 nor reset switch 24 relates to a bias portion for supplying an offset current to an input of the load portion, which converts output currents of all or part of the storing portions into corresponding voltages

in contrast to the claimed invention and as further supported in the specification at pg. 8, lines 23-28.

Further, *Kobayashi* is deficient with respect to a calculating portion for calculating an output signal of the load portion based on the voltage signal converted by the load portion. The Office Action alleges that the calculating portion (subtract circuit) for calculating an output signal of the load portion based on the voltage signal converted by the load portion is disclosed in *Kobayashi* at column 9, lines 16-25. However, this passage refers to the arrangement of two capacitors, C_{T1} and C_{T2}, to reduce a reset random noise generated when resetting a sensor accumulation terminal section with a reset transistor and an offset-fixing pattern noise generated in a source follower section. See, *Kobayashi*, column 9, lines 10-25. This application does not relate to either the calculating portion or the load portion of the claimed invention.

Based on at least these noted reasons, Applicants believe that *Kobayashi* is distinguishable with respect to the claimed invention. Therefore, Applicants respectfully submit that *Kobayashi* fails to anticipate the claimed invention.

Accordingly, Applicants respectfully request that the rejection of claims 16-33 under 35 U.S.C. § 102 be withdrawn.

For the foregoing reasons, Applicants respectfully submit that the present application is in condition for allowance and earnestly solicit reconsideration of the same.

Respectfully submitted,

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